CLAIMS

We claim:

1. A method for detecting over programming, comprising the steps of:

programming one or more multi-state storage elements associated with a first control line;

programming one or more multi-state storage elements associated with a second control line subsequent to said step of programming said one or more multi-state storage elements associated with said first control line; and

determining whether said one or more multi-state storage elements associated with said first control line are over programmed after performing said step of programming said one or more multi-state storage elements associated with said second control line.

2. A method according to claim 1, wherein:

said first control line is a first bit line; and

said second control line is a second bit line adjacent to said first bit line.

3. A method according to claim 1, wherein:

said first control line is a first word line; and

said second control line is a second word line adjacent to said first word line.

4. A method according to claim 1, further comprising the step of:

fixing data for storage elements determined to be over programmed.

5. A method according to claim 4, wherein:

said step of fixing data include lowering a threshold voltage for a particular storage element to be within the next lowest threshold distribution.

6. A method according to claim 1, wherein:

said step of determining includes detecting whether a particular storage element is over programmed due to existence of an electric field resulting from charge on a storage element adjacent to said particular storage element.

7. A method according to claim 1, wherein:

said step of determining includes detecting whether a particular storage element has a threshold voltage within any one or a set of one or more over program ranges.

8. A method according to claim 1, wherein:

said step of determining includes detecting whether a particular storage element has a threshold voltage within any one or a set of one or more over program ranges, said over program ranges are determined by estimating an effect of an electric field resulting from charge on a storage element adjacent to said particular storage element.

9. A method according to claim 1, wherein said step of determining includes performing a method comprising the steps of:

performing read operations on said multi-state storage element associated with said first control line for edges of one or more over program ranges; and

determining that a particular multi-state storage element associated with said first control line is over programmed if said particular multi-state storage element has threshold voltage within one or said one or more over program ranges, said particular multi-state storage element is adjacent to at least one of said multi-state storage elements associated with said second control line.

10. A method according to claim 9, wherein:

said first control line is a first word line; and

said second control line is a second word line.

11. A method according to claim 1, wherein said step of determining includes performing a method comprising the steps of:

performing read operations on said multi-state storage elements associated with said first control line for a set of one or more read compare points in order to determine initial states for said multi-state storage element associated with said first control line;

performing an error correction code process for said multi-state storage element associated with said first control line and said initial states; and

determining that a particular multi-state storage element associated with said first control line is over programmed if said error correction code process for said particular multi-state storage element fails, said particular multi-state storage element is adjacent to at least one of said multi-state storage elements associated with said second control line.

12. A method according to claim 11, wherein:

said first control line is a first word line; and

said second control line is a second word line.

13. A method according to claim 10, further comprising the step of:

fixing data for said particular multi-state storage if said particular multi-state storage is over programmed.

14. A method according to claim 1, wherein:

said one or more multi-state storage elements associated with said first control

line and said one or more multi-state storage elements associated with said second control line are NAND flash memory elements.

15. A method according to claim 1, wherein:

said one or more multi-state storage elements associated with said first control line are part of an array of storage elements;

said array of storage elements is on an integrated circuit chip; and

said step of determining is performed by one or more circuits on said integrated circuit chip.

16. A method for detecting over programming, comprising the steps of:

programming a first multi-state storage element;

programming a second multi-state storage element, said second multi-state storage element has an electric field that can have an effect on said first multi-state storage element, said step of programming a second first multi-state storage element is commenced after performing said step of programming said first multi-state storage element; and

determining whether said first multi-state storage element is over programmed after performing said step of programming said second multi-state storage element.

17. A method according to claim 16, wherein:

said first multi-state storage element is connected to a first word line;

said second multi-state storage element is connected to a second word line; and

said second multi-state storage element is adjacent to said first multi-state storage element.

18. A method according to claim 16, wherein:

said first multi-state storage element is part of a first NAND chain connected to a first bit line; and

said second multi-state storage element is part of a second NAND chain connected to a second word line.

19. A method according to claim 16, wherein:

said step of determining includes detecting whether said first multi-state storage element is over programmed due to existence of an electric field resulting from charge on said second multi-state storage element, said second multi-state storage element is adjacent to said first multi-state storage element.

20. A method according to claim 16, wherein said step of determining includes performing a method comprising the steps of:

performing read operations on said first multi-state storage element for edges of one or more over program ranges; and

determining that said first multi-state storage element is over programmed if said first multi-state storage element has a threshold voltage within one or said one or more over program ranges, said second multi-state storage element is adjacent to said first multi-state storage element.

21. A method according to claim 16, wherein said step of determining includes performing a method comprising the steps of:

performing read operations on said first multi-state storage element for a set of one or more read compare points in order to determine initial states for said first multi-state storage element;

performing an error correction code process for said first multi-state storage element and said initial state; and

determining said first multi-state storage element is over programmed if said error correction code process fails, said second multi-state storage element is adjacent to said first multi-state storage element.

22. A memory system, comprising:

means for programming one or more multi-state storage elements associated with a first control line;

means for programming said one or more multi-state storage elements associated with said second control line subsequent to said step of programming said one or more multi-state storage elements associated with said first control line; and

means for determining whether said one or more multi-state storage elements associated with said first control line are over programmed after performing said step of programming said one or more multi-state storage elements associated with said second control line.

23. A memory system according to claim 22, wherein means for determining includes:

means for performing read operations on said one or more multi-state storage elements associated with said first control line for edges of one or more over program ranges; and

means for determining that said one or more multi-state storage elements associated with said first control line are over programmed if said one or more multi-state storage elements associated with said first control line have a threshold voltage within one of said over program ranges.

24. A memory system according to claim 23, wherein:

said first control line is a first word line; and

said second control line is a second word line.

25. A memory system according to claim 22, wherein said means for determining includes:

means for performing read operations on said one or more multi-state storage elements associated with said first control line for a set of one or more read compare points in order to determine initial states for said first multi-state storage element;

means for performing an error correction code process for said one or more multi-state storage elements associated with said first control line; and

means for determining whether said one or more multi-state storage elements associated with said first control line are over programmed if said error correction code process fails.

26. A memory system according to claim 25, wherein:

said first control line is a first word line; and

said second control line is a second word line.

27. A memory system, comprising:

an array of multi-state storage elements; and

a managing circuit in communication with said array of multi-state storage elements, said managing circuit performs programming operations including programming one or more of said multi-state storage elements that are associated with a first control line and subsequently programming one or more of said multi-state storage elements that are associated with a second control line, said managing circuit determines whether said one or more multi-state storage elements associated with said first control line are over programmed after programming said one or more multi-state storage elements associated with said second control line, at least a subset of said multi-state

storage elements associated with said second control line are adjacent to multi-state storage elements associated with said first control line.

28. A memory system according to claim 27, wherein:

said first control line is a first bit line; and

said second control line is a second bit line adjacent to said first bit line.

29. A memory system according to claim 27, wherein:

said first control line is a first word line; and

said second control line is a second word line adjacent to said first word line.

30. A memory system according to claim 27, wherein:

said one or more multi-state storage elements associated with said first control line and said one or more multi-state storage elements associated with said second control line are NAND flash memory elements.

31. A memory system according to claim 27, wherein:

said one or more multi-state storage elements are part of an array of storage elements;

said array of storage elements is on an integrated circuit chip;

said managing circuit includes a state machine;

said state machine is on said integrated circuit chip; and

said state machine performs said determination of whether said one or more multi-state storage elements associated with said first control line are over programmed.

32. A memory system according to claim 27, wherein:

said managing circuit fixes data for storage elements determined to be over

programmed.

33. A memory system according to claim 27, wherein:

said managing circuit detects whether a particular storage element is over programmed due to existence of an electric field resulting from charge on a storage element adjacent to said particular storage element.

34. A memory system according to claim 27, wherein:

said managing circuit detects whether a particular storage element has a threshold voltage within any of a set of one or more over program ranges, said over program ranges are determined by estimating an effect of an electric field resulting from charge on a storage element adjacent to said particular storage element.

35. A memory system according to claim 27, wherein:

said managing circuit performs read operations on said multi-state storage elements associated with said first control line for edges of one or more over program ranges and determines that a particular multi-state storage element associated with said first control line is over programmed if said particular multi-state storage element has threshold voltage within one or said one or more over program ranges.

36. A memory system according to claim 35, wherein:

said first control line is a first word line; and

said second control line is a second word line adjacent to said first word line.

37. A memory system according to claim 27, wherein:

said managing circuit performs read operations on said multi-state storage elements associated with said first control line for a set of one or more read compare

points in order to determine initial states for said multi-state storage element associated with said first control line and performs an error correction code process for said multi-state storage element associated with said first control line, said managing circuit determines that a particular multi-state storage element associated with said first control line is over programmed if said error correction code process for said particular multi-state storage element fails.

38. A memory system according to claim 37, wherein:

said first control line is a first word line; and

said second control line is a second word line adjacent to said first word line.